(54) Method for attenuating spurious signals and receiver

(57) The invention relates to a method and radio receiver for attenuating spurious signals when receiving (6 to 12) radio signals, when radio signals are mixed (10) to a second frequency, which may be the baseband frequency, for example. Spurious signals are caused by balance errors in the mixer (10) which result from component value fluctuations within tolerance limits. According to the invention, mixing is balanced by setting (12) variable-level bias voltages and/or currents to transistors in the mixer circuit (10). An advantage of the invention is that even-order spurious signals caused by balance errors in the mixing of a signal to a second frequency are considerably attenuated. The invention finds particular utility in a mobile communications device; for example.
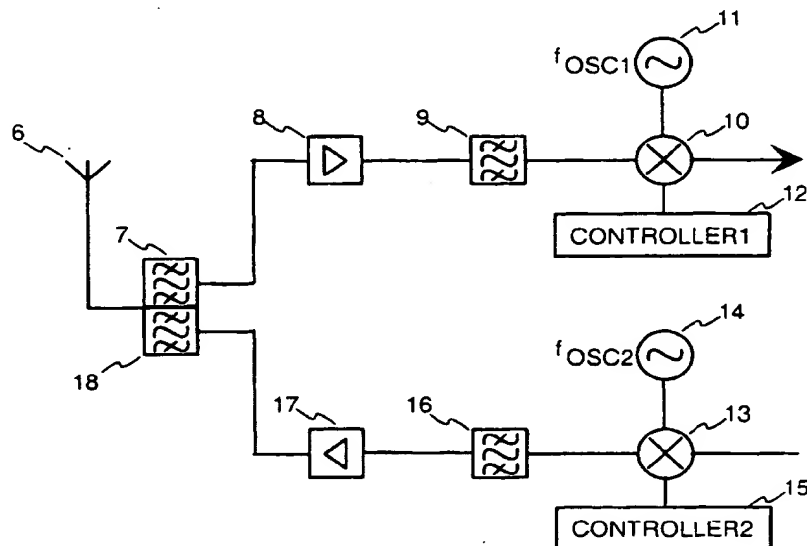
FIGURE 6

Description

[0001] The invention relates to a method for attenuating spurious signals in a transmitter and/or receiver in which radio signals are mixed to a second frequency, e. g. to an intermediate frequency (IF) or, in the case of so-called direct conversion, straight to the baseband, i.e. 0-Hz IF, and in addition the invention relates to a receiver. The invention thus pertains to a method defined in the preamble of claim 1 and a receiver defined in the preamble of claim 7.

[0002] When aiming at good linearity in radio reception, the biggest problem is usually the mixing of the received signal. Mixing is used for converting a high-frequency received signal down to a lower intermediate frequency. Attempts are made to attenuate in different ways the mixing results of even and odd orders which are brought about in the mixing in addition to the desired result. The mixing results of even orders are canceled by means of balanced or double-balanced mixer constructions. In the ideal situation, the even mixing results of two branches of a mixer cancel each other as being opposite. In practice, the attenuation caused by canceling is sufficient when the intermediate frequency is right and frequency-selective filtering is used. Then the frequencies causing the second order are attenuated already before the mixer down to a level where not too many of those frequencies will be generated in the mixer. However, there are receivers in which it is advantageous to use an intermediate frequency that might temporarily have a second-order spurious signal. Such a receiver is found e.g. in a multiple-frequency transceiver using one intermediate frequency and a common local oscillator.

[0003] Spurious responses will also be generated in a direct-conversion receiver, the worst being modulation-frequency interference at the receiver's mixer output caused by a strong amplitude-modulated (AM) signal of another transceiver. This will appear even if the frequency of the interfering signal considerably deviated from the receiving frequency. These interferences are mainly caused by the second-order distortion component which contains a variable-level DC component proportional to the amplitude of the interference-causing signal. The variable-amplitude signal produces at the mixer output a signal which comprises a variable DC component and the frequency of which is identical with the varying of the amplitude. This signal is attenuated in accordance with the mixer's balance accuracy and linearity. Sufficient attenuation can be achieved e.g. by using a mixer that has a good signal amplitude tolerance. In this way even spurious signals of a large amplitude will not cause a considerable interfering signal at the mixer output.

[0004] From the prior art it is known a so-called Gilbert cell which is widely used in integrated multiplier circuits of communications systems, especially in mobile communication devices. Multiplier circuits are used in integrated IF parts such as mixers and variable gain amplifiers.

[0005] A mixer can be based on a Gilbert cell. Such a mixer has to use large currents, high operating voltages and high local oscillator level to achieve a small relative portion of interfering signal and small effect on the mixer operating points. Additionally, the balance of the incoming RF signal, balance of the amplification of the different branches of the mixer, and the balance of the local oscillator are of great importance to the attenuation of spurious signals of even orders. The low voltage used nowadays because of the tendency to reduce power consumption causes that not all mixer types provide sufficient attenuation of spurious signals. Tolerances of the components used in the mixers are too wide to achieve a balance good enough at low voltages.

[0006] It is a problem with known radio receivers that single unbalanced mixers produce, in addition to the desired mixing result, spurious signals of both even and odd orders.

[0007] It is another problem with known radio receivers that spurious signals of even orders, which are generated in balanced mixers in addition to the desired mixing result, are insufficiently attenuated at low voltages.

[0008] It is an object of the invention to improve the attenuation of spurious signals of even orders so that an adequate end result will be achieved even with low operating voltages and smaller currents.

[0009] The method according to the invention is characterized by what is expressed in claim 1. The receiver according to the invention is characterized by what is expressed in claim 7. Preferred embodiments of the invention are described in the dependent claims.

[0010] The invention pertains to a method for attenuating spurious signals in a transmitter and/or receiver in which radio signals are mixed to a second frequency which may also be the baseband frequency. In accordance with the invention, mixing is balanced by adjusting transistor bias voltages and/or currents in the mixer circuit.

[0011] The invention also pertains to a receiver that comprises a mixer for mixing radio signals to a second frequency, which may also be the baseband frequency, and means for attenuating spurious signals while receiving radio signals. In accordance with the invention, it comprises balance-adjusting means of mixer circuit to adjust the balance of the circuit by adjusting transistor bias voltages and/or currents in the mixer circuit.

[0012] It is an advantage of the invention that in the mixing to a second frequency spurious signals of even orders caused by balance errors resulting from component tolerances are considerably attenuated.

[0013] The invention will now be described in more detail with reference to the accompanying drawing wherein

Fig. 1   shows in the form of circuit diagram a known Gilbert cell.

Fig. 2   shows in the form of flow diagram a method according to the invention for adjusting the balance of a mixer,

Fig. 3   shows, in the form of circuit diagram a bias voltage adjustment block of a mixer according to the invention,

Fig. 4   shows in the form of circuit diagram a mixer according to the invention,

Fig. 5   shows in the form of circuit diagram a radio-frequency stage according to the invention,

Fig. 6   shows in the form of block diagram essential parts of a transceiver according to the invention, and

Fig. 7   shows in the form of block diagram a control-ler according to the invention for controlling an adjustment block.

[0014]   Fig. 1 shows a known Gilbert cell used for re-alizing integrated IF parts such as variable gain ampli-fiers and mixers. In a Gilbert cell two input voltages are multiplied into one output voltage, i.e. the voltage differ-ence at the outputs is the product of the differences in the input voltages. A first voltage difference is coupled to terminals V_{X+} and V_{X-} wherefrom the voltages are tak-en to the bases of transistors Q3, Q4 and Q6, Q7, re-spectively. A second voltage difference is coupled to ter-minals V_{Y+} and V_{Y-} wherefrom the voltage is amplified by transistors Q5 and Q8. Transistors Q5 and Q8 are coupled through resistors R_{E1} and R_{E2} to a field effect transistor (FET) Q9 which is controlled by a bias voltage V_{BIAS} and coupled to a negative operating voltage. Tran-sistors Q3 and Q7 amplify a positive voltage difference V_{X+} and V_{X-}, and the amplified voltage difference is cou-pled to outputs V_{OUT+} and V_{OUT-}. The circuit mentioned above is coupled to a positive operating voltage through resistors R_{L1} and R_{L2}. Transistors Q2 and Q4 amplify a negative voltage difference V_{X+} and V_{X-}, and the ampli-fied voltage difference is crosscoupled to outputs V_{OUT+} and V_{OUT-}.

[0015]   Fig. 2 shows in the form of flow diagram a bal-ance adjustment method for a mixer according to the invention. First, possible previous bias voltages 1 are removed. Then, the balance error 2 of the mixer is de-termined by coupling a radio signal to the receiver in-puts, thus causing a spurious signal in the mixer, which is then measured at the mixer outputs. Next, a bias volt-age 3 correcting the balance error is set, preferably by feeding an inversely proportional CTRL byte corre-sponding to the error to the adjustment block by means of a digital controller. If the error-correcting bias voltage cannot be determined on the basis of the measurement result, a trial bias voltage is set. CTRL byte means a binary number that sets the control for the CTRL lines. The binary lines of the CTRL byte control the switching transistors in the adjustment block, so that I_{BIAS} is changed and the voltages between the terminals of the bias resistors change. The potential of the operating point of the mixer's transistor input is adjusted according

to the point between the bias resistors. In other words, the adjustment block forms a variable voltage across the resistor in the series connection when the adjustment is carried out by means of current. The adjustment block may also be implemented using a variable voltage source. The operational input signals of the transistors are alternating voltages conducted by a capacitive com-ponent. When the bias voltage that corrects or at least changes the balance error has been generated, it is checked whether the error correction was successful, i. e. whether the mixer is in balance 4. If not, operation returns to step 2 to determine the remaining error and change the bias voltages on the basis of that determi-nation. If the setting of the bias reduced the balance er-ror, the bias is increased, but if the balance error became bigger the bias is taken back towards zero or, if zero is reached, the bias is set on the second line of the input pair. Thus, bias voltage remains advantageously only on one of the lines of the input pair in the balanced state. When the balancing has succeeded, the data of the bal-ancing controller are stored in memory and normal op-eration of the mixer is started 5.

[0016]   Fig. 3 shows in a circuit diagram an adjustment block for the bias voltage of a mixer according to the invention. In the adjustment block, a current from a ref-erence current source I_{REF} flows via a transistor Q_{REF} from the operating voltage VDD to ground. Current I_{REF} is mirrored to a bias current circuit on the right. Current I_{BIASB} through transistor Q_{BIASB} constitutes the invaria-ble fundamental part of bias current I_{BIAS}. Transistors Q1, Q2, ... QN and Q1S, Q2S, ... QNS make up N parallel series connections, and a sum current of I_1, I_2, ... I_N through said series connections constitutes the variable part of bias current I_{BIAS}. Control lines CTRL 1, 2, ... N control transistors Q1S, Q2S, ... QNS serving as switch-es. Transistors Q1, Q2, ... QN are mutually binarily weighted such that transistors Q1S, Q2S, ... QNS, which are controlled by control lines CTRL 1, 2, ... N and connected in series with said transistors, can raise cur-rent I_{BIAS} by 2^N-1 levels, which means the current gets 2^N values. Binary weighting of the currents is achieved e.g. by connecting transistors in parallel in such a way that Q1 comprises one transistor, Q2 comprises two transistors, etc. With field effect transistors (FET), the currents may also be set by selecting the channel widths. The currents are weighted preferably according to the following series: 1, 2, 4, 8, etc., i.e. 2^N, where N ≥ 0. For example, current I_1 is $I_{REF}/200$, current I_2 is $I_{REF}/100$ and I_N is $I_{REF}/(200/2^{N-1})$.

[0017]   Thus the imbalance caused by the tolerances of mixer components can be balanced using the variable part I_1, I_2, ... I_N of current I_{BIAS}. Also, possible small im-balance of input signals can be balanced using the ar-rangement according to the invention. By changing the number of control lines and the current I_{REF} of the ref-erence current source it is possible to adapt the bias adjustment steps and range to various couplings.

[0018]   Fig. 4 shows in a circuit diagram a mixer ac-

cording to the invention. In the upper left corner of Fig. 4 there are four blocks depicted in Fig. 3 that generate the bias current I_{BIAS} to control the bias voltage. The blocks are for local oscillator signal pair V_{LO+} and V_{LO-} and radio-frequency signal pair V_{RF+} and V_{RF-}, which control through capacitive elements C1 and C2 as well as C3 and C4 the transistors Q10, Q11, Q13, Q14 and Q12, Q15. Blocks BLO+, BLO-, BRF+ and BRF- are used to produce currents and, thus, voltages to four parallel bias resistor series connections R_{B1} and R_{B2}, R_{B3} and R_{B4}, R_{B5} and R_{B6} as well as R_{B7} and R_{B8}.

[0019] If the adjustment block current I_{BIAS} is the same as the necessary base current of the corresponding transistor, e.g. a beta-compensated base current, a resistor connected to ground is not used with that adjustment block. For example, if adjustment blocks BRF+ and BRF- feed the base current of transistors Q15 and Q12, resistors R_{B6} and R_{B8} are left out and the corresponding bias voltage is set by adjusting the base current.

[0020] Load impedances Z_{L3}, Z_{L4}, transistors Q10, Q11, Q12, Q13, Q14, Q15 and emitter impedances Z_{E3}, Z_{E4} constitute a known mixer the outputs of which give signals V_{OUT+} and V_{OUT-}.

[0021] The balance is adjusted preferably as described above, but the most perfect balance is achieved by adjusting the bias voltages of the transistor pair's mutually corresponding transistors Q10, Q11 and Q13, Q14 separately. In other words, the controls of the transistors that get their control from the same line, such as Q10 and Q14, are separated from each other and the bias voltages of them both are adjusted individually.

[0022] Fig. 5 shows in a circuit diagram a radio-frequency amplifier stage according to the invention which also can be used to correct a mixer's balance error. In the upper left corner of Fig. 5 there are two blocks depicted in Fig. 3 that generate the bias current I_{BIAS} to control the bias voltage. The blocks are for a radio-frequency signal pair V_{RF+} and V_{RF-} which control through capacitive elements C5 and C6 transistors Q16 and Q17. Blocks BRF+ and BRF- are used to produce currents and, thus, voltages to two parallel bias resistor series connections R_{B9}, R_{B10} and R_{B11}, R_{B12}.

[0023] Load impedances Z_{L5}, Z_{L6}, transistors Q16, Q17; emitter impedances Z_{E5}, Z_{E6} and current source I_{DIFF} constitute a known radio-frequency amplifier stage.

[0024] The circuit according to Fig. 5 described above can also be used as local oscillator buffer. Then the balance error of the local oscillator port can be corrected by adjusting the buffer.

[0025] Fig. 6 shows in the form of block diagram essential parts of a transceiver according to the invention. The transceiver shares a common antenna 6 from which a signal is received and filtered by a bandpass filter 7 and amplified by an amplifier 8 and refiltered 9. Then the signal at the radio reception frequency is mixed to an intermediate frequency in a balanced mixer 10 ac-

cording to the invention. A local oscillator 11 feeds the mixer 10 at the frequency of f_{OSC1}. The balance of the mixer 10 is adjusted by a controller 12. From the intermediate frequency on the reception continues in accordance with the prior art.

[0026] A signal to be transmitted is modulated at the local oscillator 14 frequency f_{OSC2} by means of a modulator 13. The balance of the modulator 13 is adjusted by a controller 15. The modulated signal is bandpass-filtered by a filter 16 and amplified by an amplifier 17 and filtered again by a filter 18 and fed to the antenna 6. Otherwise the transmitter is preferably realized according to the prior art, and this document does not take a position on the use of balancing according to the invention in it.

[0027] Fig. 7 shows in a block diagram essential components of a controller of an adjustment block according to the invention. The processor 20 of a digital controller is stepped by an oscillator 19 at frequency f_{PRO}. The controller executes a program from memory 21, which preferably is both read only memory (ROM) and random access memory (RAM). Measurement data on the balance is obtained by means of an A/D converter 22. Bias voltages are controlled by a D/A converter 23 which preferably comprises an adjustment block according to Fig. 3 in which current is switched by means of digital binary control to adjust the bias voltages.

[0028] For example, let us consider a radio receiver the spurious response of which is to be reduced. The receiver is adjusted preferably only once before use. A test signal is coupled to the receiver input, and the interfering signal level is measured from the receiver output. The test signal is generated in such a way that it produces a spurious response to be minimized. A trial setting is chosen e.g. for the adjustment block BRF+ of the positive line of the RF input, and the interfering signal level is measured again. If the interference was reduced, an optimum setting is found for the adjustment block BRF+ by experimental bracketing, and if the interference got worse, the initial state is restored for the adjustment block BRF+ and a trial setting is chosen for the adjustment block BRF- of the negative line of the RF input and an optimum setting is found for it by experimental bracketing. The same experimental bracketing is also carried out for the local oscillator input by adjustment blocks BLO+ and BLO-. For a good result, both bracketing tunings are repeated. Thanks to the second tuning, a possible residual error, which is not noticed at the first time because it is hidden by an error in one of the input pairs, is corrected. Tuning data for the balance achieved through the minimization of spurious response are stored in the memory of the apparatus wherefrom they can be loaded by means of a microprocessor or digital signal processor (DSP) always on start-up. Fuses, microswitches, programmable gate circuits and the like can also be used for the immediate control of the adjustment block.

[0029] Of course, the selection of the bias voltage in-

itial setting line and the level of the setting can also be realized as a preferably calculatory value based on interference measurement data. Empirical knowledge can also be utilized when estimating the bias voltage value on the basis of the measurement result.

[0030] In digital mobile communications devices, such as mobile stations operating in GSM, PCN (Personal Communication Network), DAMPS (Digital Advanced Mobile Phone Standard) or CDMA (Code Division Multiple Access) networks, the received signal is converted digital. In these apparatus the method is advantageously applied in such a way that the spurious response is measured, adjusted as small as possible, and the settings are stored in memory by carrying out the necessary routines with a digital signal processor. Then the tuning is particularly fast as it is carried out by coupling a test signal to the antenna and executing a tuning program. The adjustment blocks are controlled by a microprocessor or preferably with the same digital signal processor. A serial or parallel bus is used for the control. For a serial bus an adjustment block needs a separate logic to control the transistors.

[0031] The balance can also be tuned without a test signal while the local oscillator is operating. To that end, a comparative element is coupled to the mixer outputs to compare the voltage difference of the output pair. Particularly the DC component is compared. Tuning is performed by decreasing the voltage difference to its minimum value. However, because of bias voltages in the comparative element itself, the inputs of the comparative element must switch places and the comparison has to be repeated. The average of the tunings gives a result which is as accurate as possible. However, this tuning result is not as accurate as the one achieved using a test signal. If this type of tuning is accurate enough for the application, the tuning can be carried out automatically with a digital signal processor.

[0032] The principles according to the invention can also be utilized in the balancing of passive mixers.

[0033] The exemplary adjustment block was here realized by field effect transistors but the circuit can also be realized using bipolar transistors, for example.

[0034] The invention is not limited to the exemplary embodiments described above but many modifications are possible within the scope of the inventional idea defined by the claims set forth below.

Claims

1. A method for attenuating spurious signals in a transmitter and/or receiver in which radio signals are mixed to a second frequency which may also be the baseband frequency, **characterized** in that the mixing is balanced by adjusting bias voltages (3) and/or currents in transistors of the mixer circuit.

2. The method of claim 1, **characterized** in that the

bias voltages (3) and/or currents are adjusted in an input circuit of a radio-frequency signal.

3. The method of claim 1 or 2, **characterized** in that the bias voltages (3) and/or currents are adjusted in an input circuit of a local oscillator.

4. The method of claim 1, 2 or 3, **characterized** in that the bias voltages (3) and/or currents are adjusted separately for both transistors of a transistor pair of a signal line in the mixer circuit.

5. The method of any one of the preceding claims 1 to 4, **characterized** in that the adjustment of the bias voltages (3) and/or currents is performed using a digital-to-analog converter to adjust current I_{BIAS} for the signal line across parallel resistors.

6. The method of any one of the preceding claims 1 to 5, **characterized** in that the bias voltages (3) and/or currents are adjusted by tuning the receiver by measuring (2) the balance from the receiver outputs and empirically adjusting the bias voltages (3) and/or currents on the basis of measurements (4).

7. A receiver comprising a mixer (10) for mixing radio signals to a second frequency which may also be the baseband frequency, and means for attenuating spurious signals, when receiving radio signals, **characterized** in that it comprises balance adjustment means (12) in the mixer circuit (10) to adjust the circuit's balance by adjusting bias voltages and/or currents in transistors (Q10, Q11, Q12 Q13, Q14, Q15) of the mixer circuit.

8. The receiver of claim 7, **characterized** in that the adjustment means (12) comprises an input circuit $(V_{RF+}, V_{RF-}, C3, C4)$ for a radio-frequency signal to adjust bias voltages and/or currents of an adjustment circuit (BRF+, BRF-, R_{B5}, R_{B6}, R_{B7}, R_{B8}).

9. The receiver of claim 7 or 8, **characterized** in that the adjustment means (12) comprises a local oscillator input circuit $(V_{LO+}, V_{LO-}, C1, C2)$ to adjust bias voltages and/or currents of an adjustment circuit (BLO+, BLO-, R_{B1}, R_{B2}, R_{B3}, R_{B4}).

10. The receiver of claim 7, 8 or 9, **characterized** in that the adjustment means (12) comprises an adjustment circuit separately for both transistors of a transistor pair (Q10, Q14; Q11, Q13) of a signal line (V_{LO+}, V_{LO-}) of the mixer circuit (10) to adjust bias voltages and/or currents.

11. The receiver of any one of the preceding claims 7 to 10, **characterized** in that the adjustment means comprises a digital-to-analog converter (19) to adjust bias voltages and/or currents with a digital con-

troller (12).

12. The receiver of any one of the preceding claims 7 to 11, **characterized** in that it further comprises

- an A/D converter (18) to measure the balance,

- a D/A converter (19) to adjust bias voltages and/or currents, and

- an oscillator (15), a processor (16) and memory (17) to carry out balance measurement routines as well as bias voltage and/or current adjustment routines.
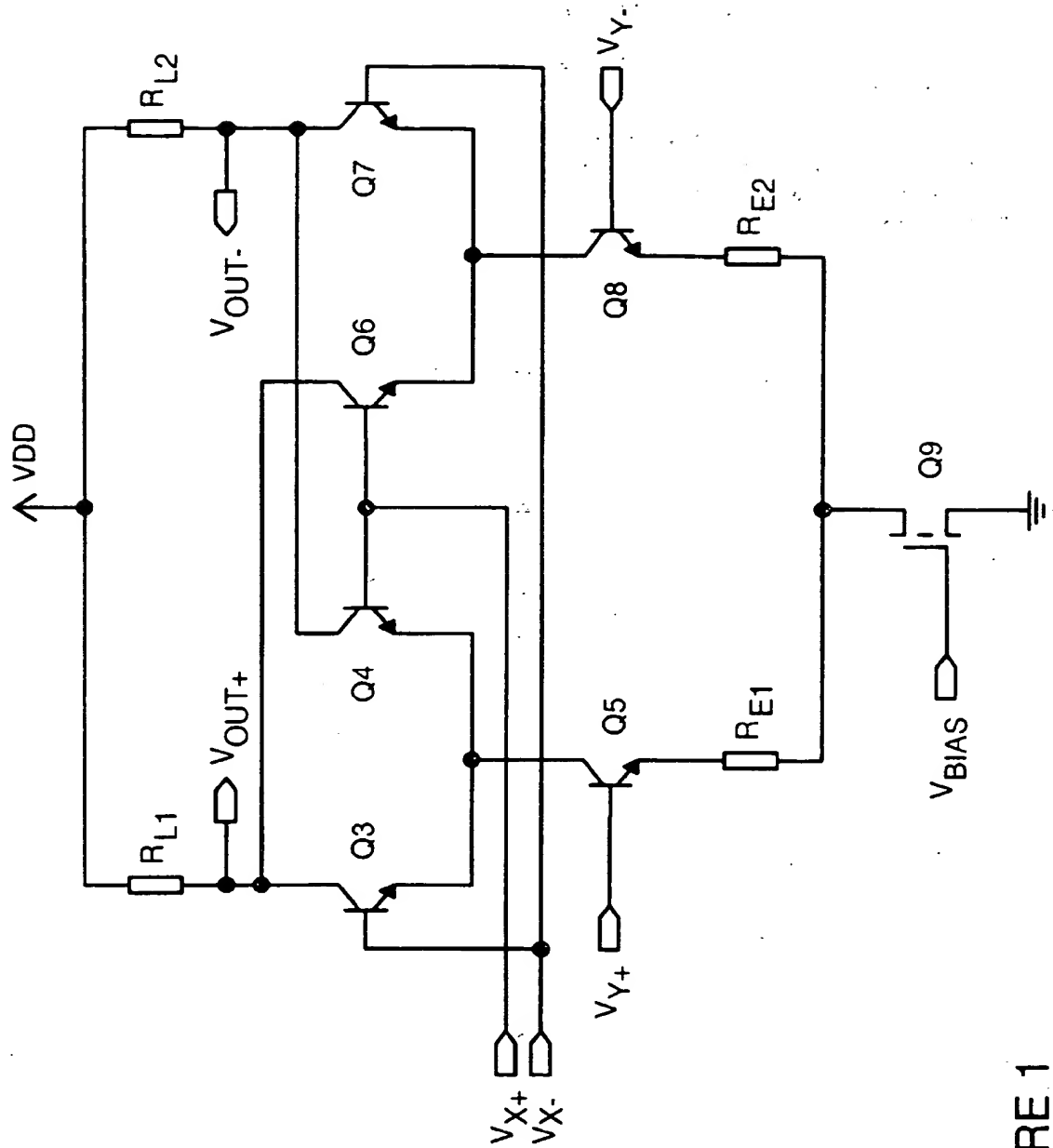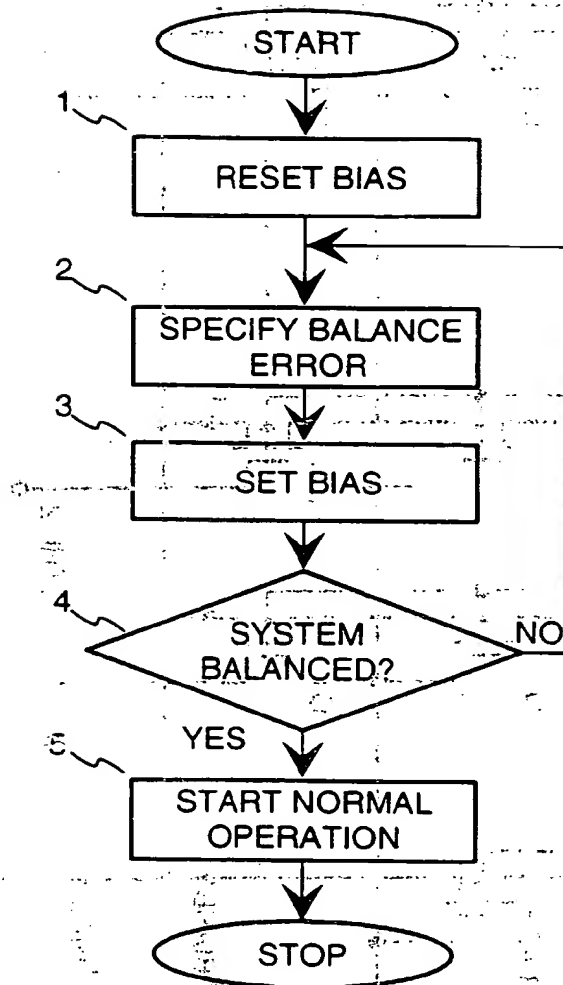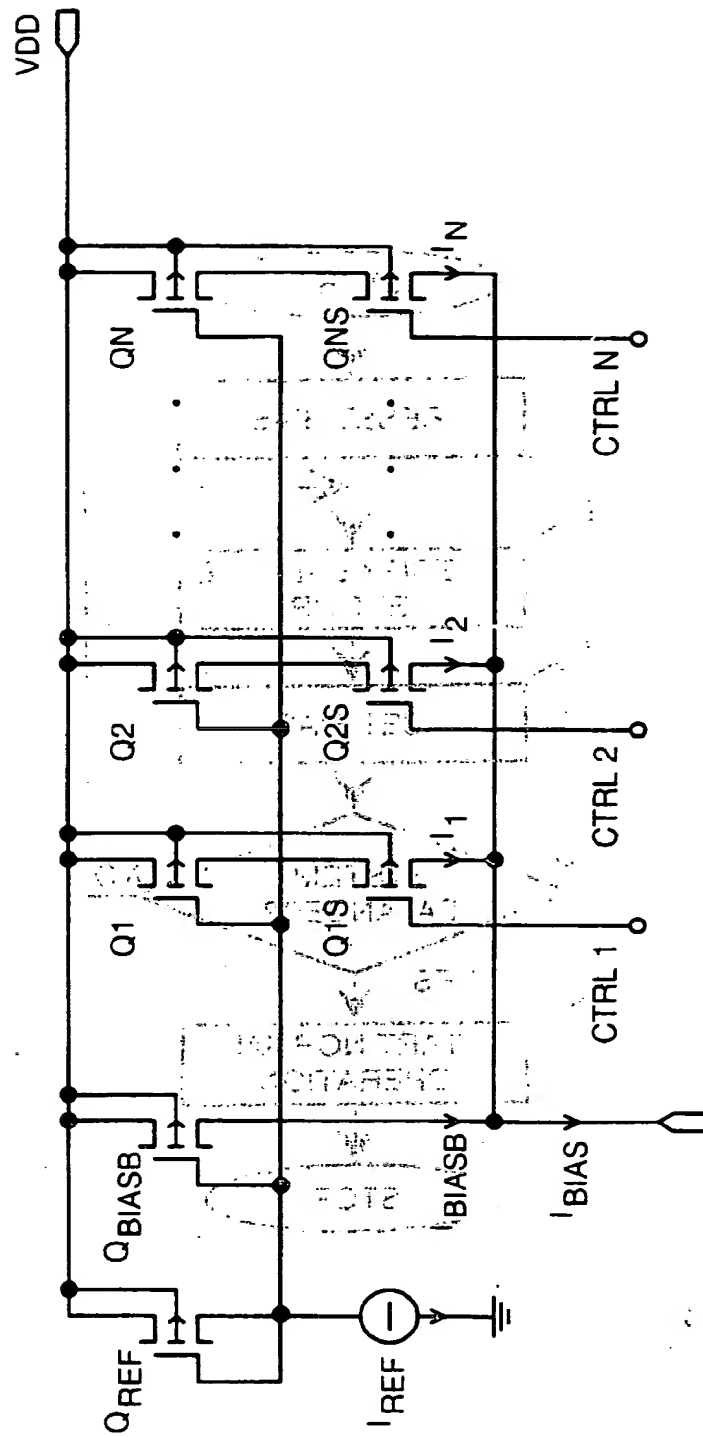
FIGURE 1

7

START

1 — RESET BIAS

2 — SPECIFY BALANCE ERROR

3 — SET BIAS

4 — SYSTEM BALANCED?   NO

YES

5 — START NORMAL OPERATION

STOP

FIGURE 2

8

FIGURE 3

9

FIGURE 4

10
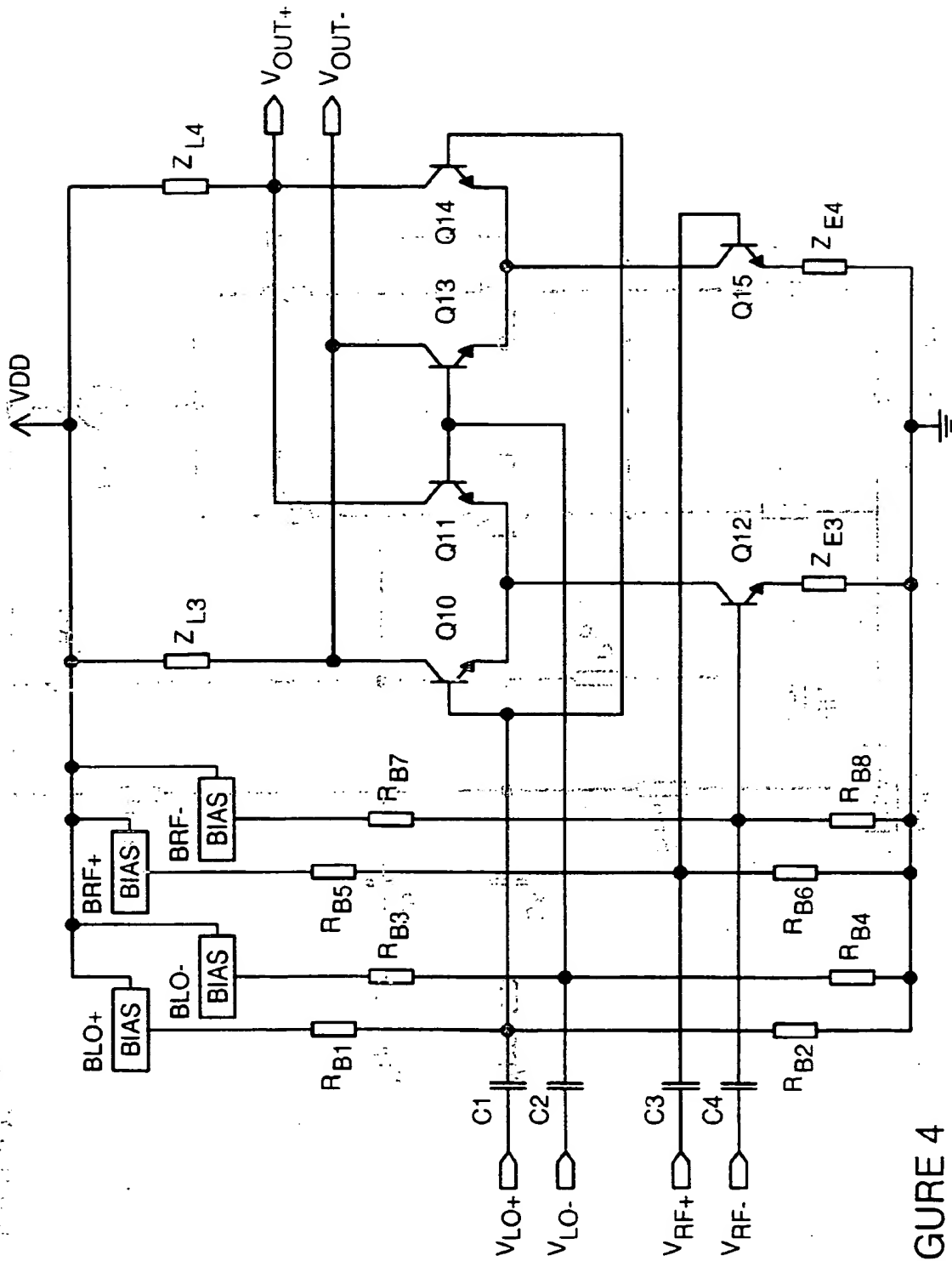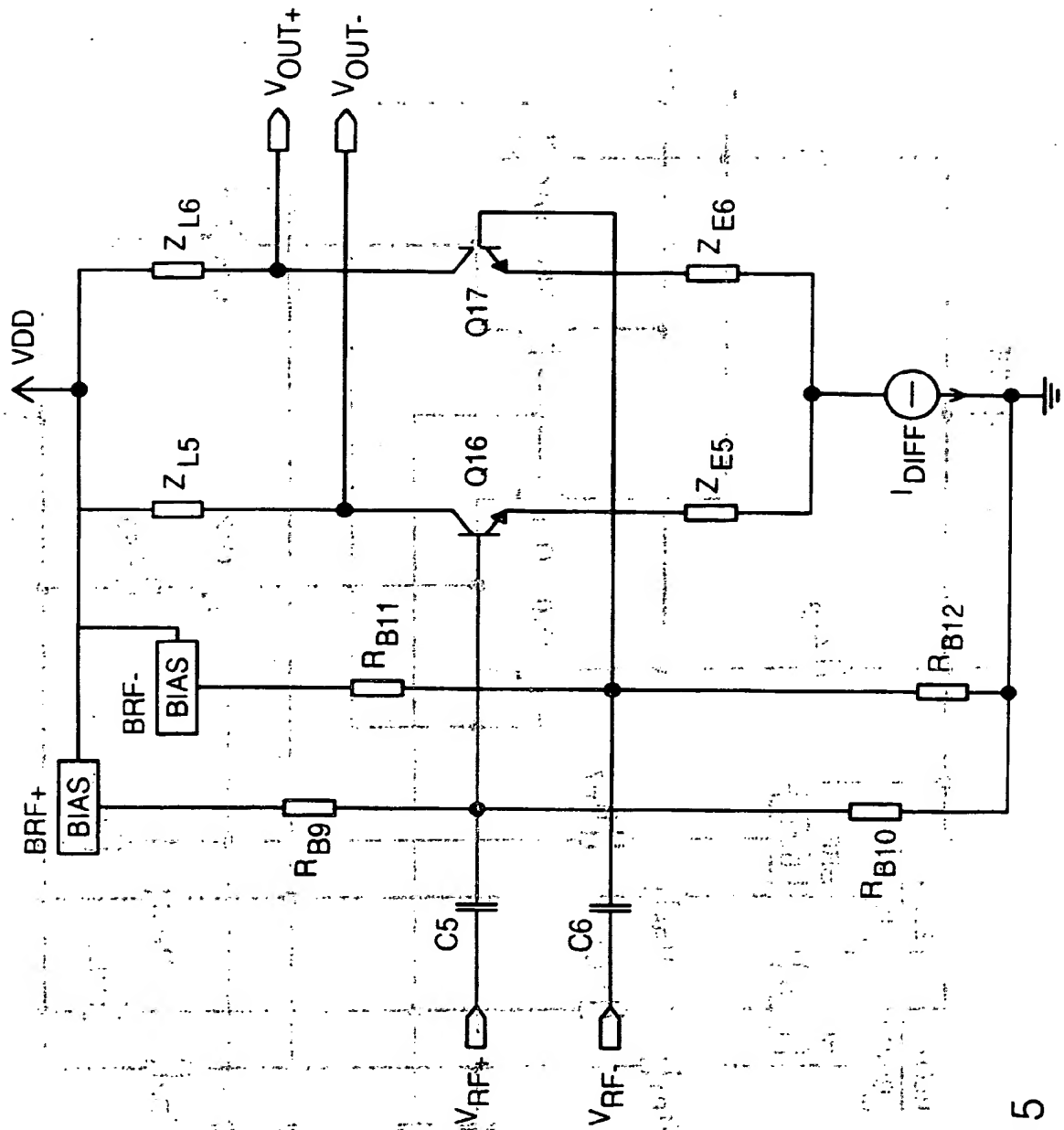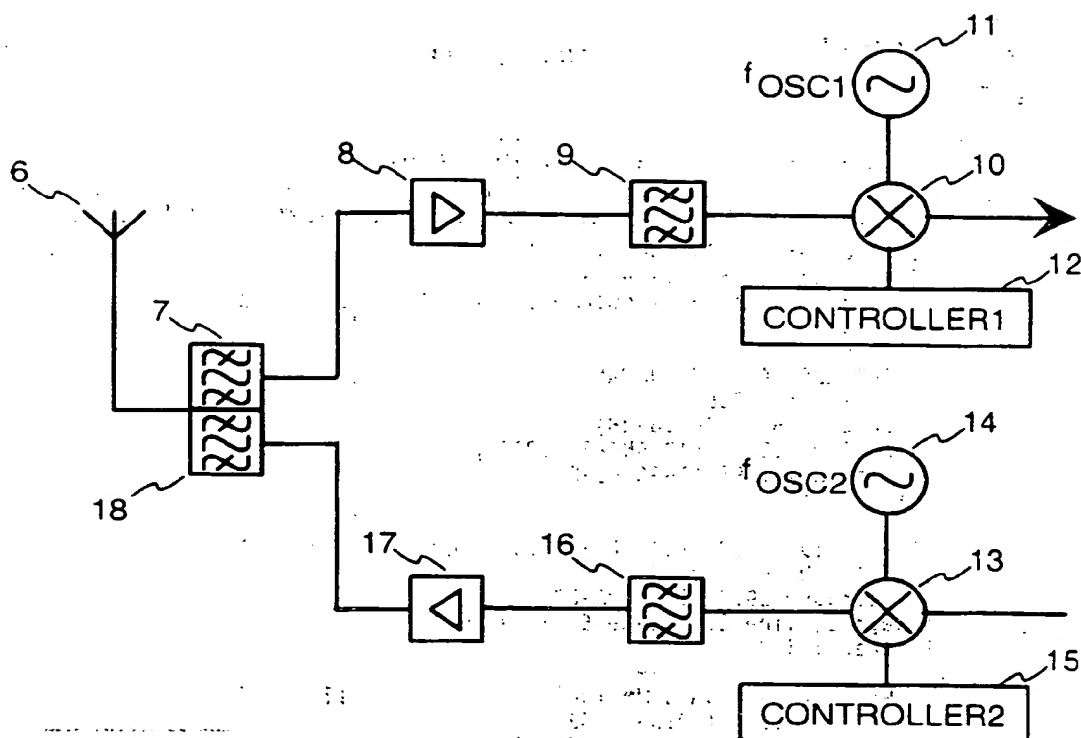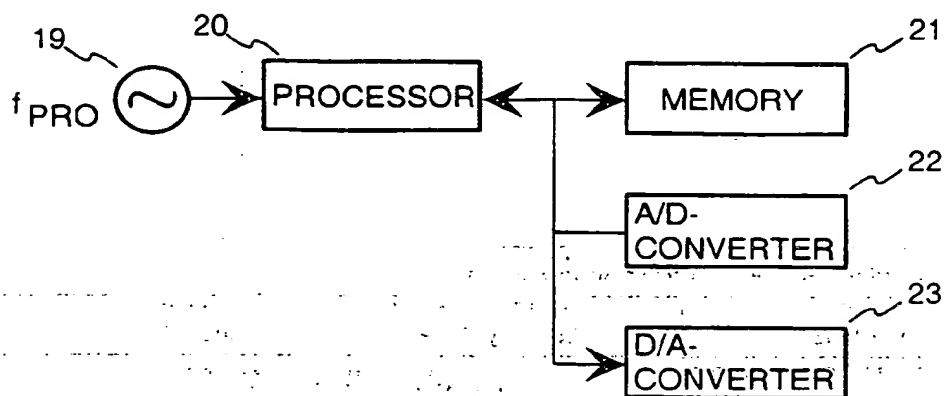
FIGURE 5

FIGURE 6

FIGURE 7

EUROPEAN SEARCH REPORT

European Patent Office

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	US 5 584 066 A (OKANOBU TAIWA) 10 December 1996 (1996-12-10)	1,6,7	H03D7/14
Y	* column 4, line 56 - column 9, line 45; figures 4,7,8 *	2-5,8-12	
Y	PATENT ABSTRACTS OF JAPAN vol. 096, no. 006, 28 June 1996 (1996-06-28) & JP 08 056121 A (ADVANTEST CORP), 27 February 1996 (1996-02-27) * abstract *	2,5,8,11	
Y	WO 97 07596 A (PHILIPS ELECTRONICS NV ;PHILIPS NORDEN AB (SE)) 27 February 1997 (1997-02-27) * page 1, line 21 - page 6, line 26; figures 1,3 *	3,4,9,10	
Y	WO 95 30275 A (QUALCOMM INC) 9 November 1995 (1995-11-09) * page 17, line 3 - page 18, line 17; figure 9 *	12	
A	PIAZZA F ET AL: "A 170 MHZ RF FRONT-END FOR ERMES PAGER APPLICATIONS" IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 30, no. 12, 1 December 1995 (1995-12-01), pages 1430-1437, XP000557248 ISSN: 0018-9200		

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H03D
H04B
H03C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 July 1999	Dhondt, I

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.   EP 99 66 0061

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

16-07-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5584066 A	10-12-1996	JP 7111471 A	25-04-1995
		CN 1118535 A	13-03-1996
JP 08056121 A	27-02-1996	NONE	
WO 9707596 A	27-02-1997	EP 0801849 A	22-10-1997
		JP 10507894 T	28-07-1998
WO 9530275 A	09-11-1995	AT 164974 T	15-04-1998
		AU 694514 B	23-07-1998
		AU 2398995 A	29-11-1995
		BR 9566205 A	23-04-1996
		CA 2163883 A	09-11-1995
		CN 1128091 A	31-07-1996
		DE 69501996 D	14-05-1998
		DE 69501996 T	15-10-1998
		EP 0706730 A	17-04-1996
		ES 2115380 T	16-06-1998
		FI 956286 A	26-02-1996
		HK 1005920 A	29-01-1999
		JP 8510892 T	12-11-1996
		SI 706730 T	31-12-1998
		US 5617060 A	01-04-1997
		ZA 9500605 A	20-12-1995